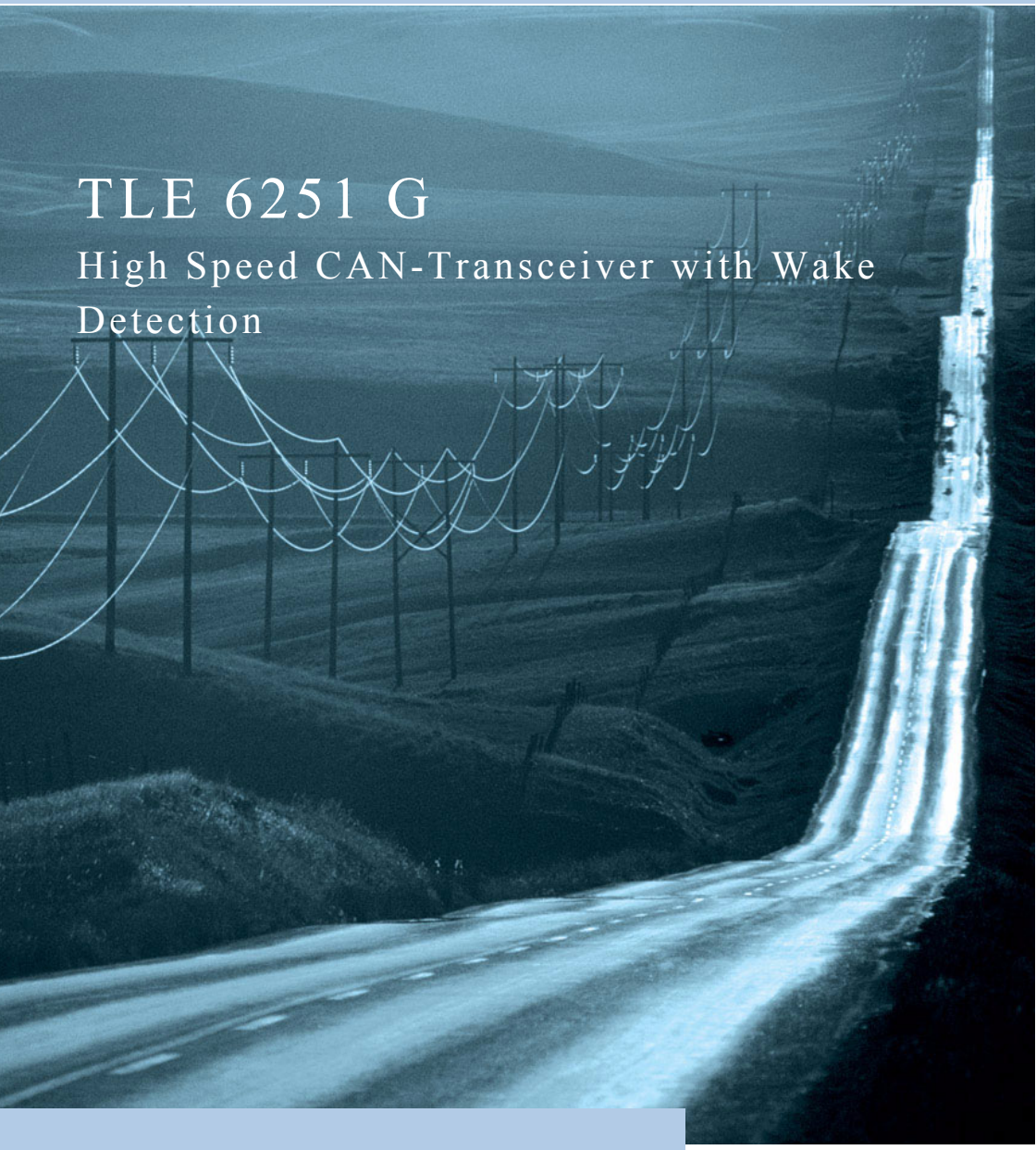

TLE 6251 G

High Speed CAN-Transceiver with Wake Detection

Automotive Power

Never stop thinking.

Edition 2008-06-19

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81669 München, Germany

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Features

P-DSO-14-13

- CAN data transmission rate up to 1 Mbaud
- Compatible to ISO/DIS 11898
- Supports 12 V and 24 V automotive applications
- Low power modes with local wake-up input and remote wake-up via CAN bus
- Very low power consumption in sleep mode
- Wake-up input
- Wake-up source recognition
- Inhibit output to control an external power supply
- Diagnosis output
- RxD only mode for node failure analysis
- Split termination to stabilize the recessive level
- TxD time-out function with diagnosis
- RxD recessive clamping handler with diagnosis
- TxD to RxD short circuit handler with diagnosis
- Bus line short circuit diagnosis
- Bus dominant clamping diagnosis
- Undervoltage detection at V_{CC}, $V_{I/O}$ and V_{BAT}
- Cold start diagnosis (first battery connection)
- Adaptive to host logic supply levels (3.3 and 5 V)
- Wide common mode range for electromagnetic immunity (EMI)
- Low electromagnetic emission (EME)
- Short circuit proof to ground, battery and V_{CC}
- Overtemperature protection
- Protected against automotive transients
- +/- 6kV ESD Robustness according to IEC 61000-4-2

Type	Ordering Code	Package
TLE 6251 G	On Request	P-DSO-14-13

Description

The CAN-transceiver TLE 6251 G is a monolithic integrated circuit in a P-DSO-14-13 package for high speed differential mode data transmission (up to 1 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO/DIS 11898.

As a successor to the first generation of HS CAN, the TLE 6251 G is designed to provide an excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications). The current consumption can be reduced, due to the low power modes.. This supports networks with partially powered down nodes.

The TLE 6251 G offers two low power modes as well as a receive-only mode to support software diagnosis functions. A wake-up from the low power mode is possible via a message on the bus or via the bi-level sensitive wake input. An external voltage supply IC can be controlled by the inhibit output. So, the µC can be powered down and the TLE 6251 G still reacts to wake-up activities on the CAN bus or local wake input.

A diagnosis output allows mode dependent enhanced diagnosis of bus failures and wake-up source. A V_{BAT} fail flag reports an power-on condition at the battery supply input.

The TLE 6251 G is designed to withstand the severe conditions of automotive applications and to support 12 V and 24 V applications.

The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

Pin Configuration

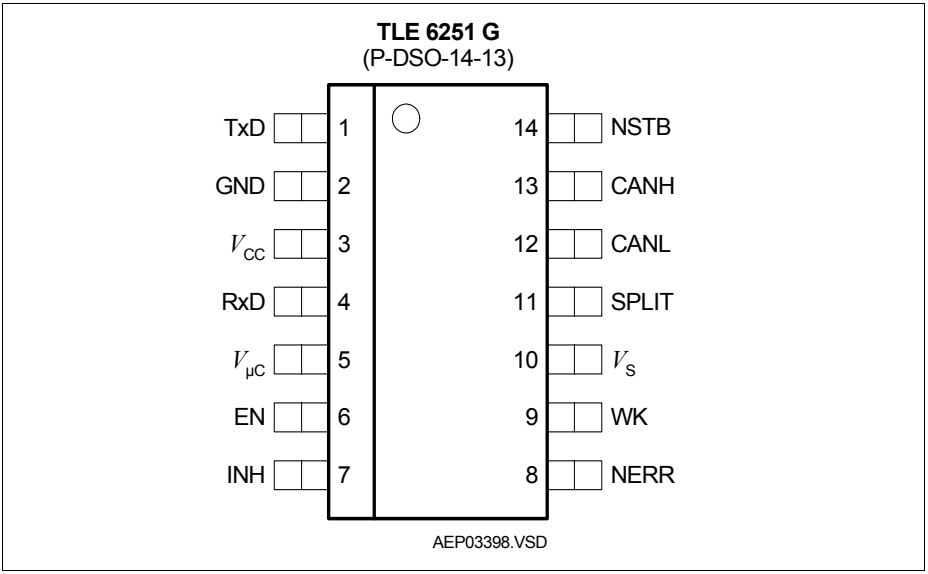


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	TxD	**CAN transmit data input;** 20 kΩ pull-up, LOW in dominant state
2	GND	**Ground**
3	V_{CC}	**5 V supply input;** block to GND with 100 nF ceramic capacitor
4	RxD	**CAN receive data output;** LOW in dominant state, push-pull output stage
5	$V_{\mu C}$	**Logic voltage level adapter input;** connect to pin V_{CC} for 5 V microcontroller, connect to additional supply voltage for other logic voltage levels, block to GND with 100 nF ceramic capacitor
6	EN	**Mode control input 1;** internal pull-down, see **Figure 6**
7	INH	**Control output;** set HIGH to activate voltage regulator; open drain
8	NERR	**Diagnosis output 1;** error and power on indication output, push-pull output stage
9	WK	**Wake-up input;** bi-level sensitive

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
10	V_S	**Battery voltage supply input;** block to GND with 100 nF ceramic capacitor
11	SPLIT	**Termination output;** to support the recessive voltage level of the bus lines (see **Table 2**)
12	CANL	**Low line output;** LOW in dominant state
13	CANH	**High line output;** HIGH in dominant state
14	NSTB	**Mode control input 2;** internal pull-down, see **Figure 6**

Functional Block Diagram

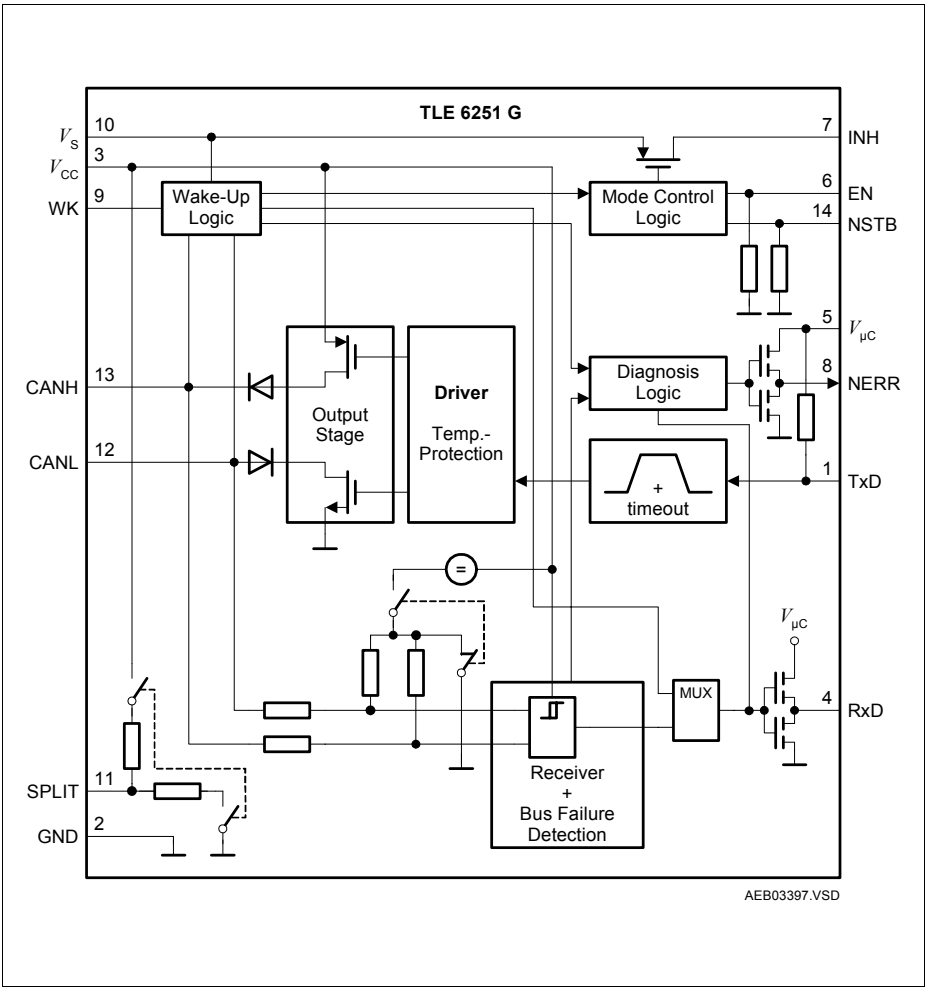


Figure 2 Block Diagram

Application Information

As a successor to the first generation of HS CAN, the TLE 6251 G is designed to provide an excellent passive behavior when the transceiver is switched off (mixed networks, terminal 15/30 applications). The current consumption can be reduced, due to the low power modes. This supports networks with partially powered down nodes.

A wake-up from the low power modes is possible via a message on the bus or via the bi-level sensitive wake input WK. An external voltage supply IC can be controlled by the inhibit output INH. So, the µC can be powered down and the TLE 6251 G still reacts to wake-up activities on the CAN bus or local wake input activities.

A diagnosis output pin NERR, allows mode dependent enhanced diagnosis of bus failures and wake-up source. A V_{BAT} fail flag reports a power-on condition at the battery supply input. The V_{BAT} fail flag will be resetted after the first transition into normal mode.

The TLE 6251 G has four operation modes, the normal, the receive only, the standby mode and the sleep mode. These modes can be controlled with the two control pins EN and NSTB pin (see **Figure 6**, **Table 2**). Both, EN and NSTB, have an implemented pull-down, so if there is no signal applied to EN and NSTB, the transceiver automatically changes to the standby mode.

Normal Mode

To transfer the TLE 6251 G into the normal mode, NSTB and EN have to be switched to HIGH level. This mode is designed for the normal data transmission/reception within the HS-CAN network.

Transmission

The signal from the µC is applied to the TxD input of the TLE 6251 G. Now the bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

TxD Time-out Feature

If the TxD signal is dominant for a time $t > t_{TxD}$, the TxD time-out function deactivates the transmission of the signal at the bus. This is realized to prevent the bus from being blocked permanently due to an error.

The transmission is released again, after a mode state change.

TxD to RxD Short Circuit Feature

Similar to the TxD time-out, a TxD to RxD short circuit would also drive a permanent dominant signal at the bus and so block the communication. To avoid this, the TLE 6251 G has a TxD to RxD short circuit detection.

Reduced Electromagnetic Emission

The bus driver has an implemented control to reduce the electromagnetic emission (EME). This is achieved by controlling the symmetry of the slope, resp. of CANH and CANL.

Overtemperature

The driver stages are protected against overtemperature. Exceeding the shutdown temperature results in deactivation of the driving stages at CANH/L. To avoid a bit failure after cooling down, the signals can be transmitted again only after a dominant to recessive edge at TxD.

Figure 3 shows the way how the transmission stage is deactivated and activated again. First an overtemperature condition causes the transmission stage to deactivate. After the overtemperature condition is no longer present, the transmission is only possible after the TxD bus signal has changed to recessive level.

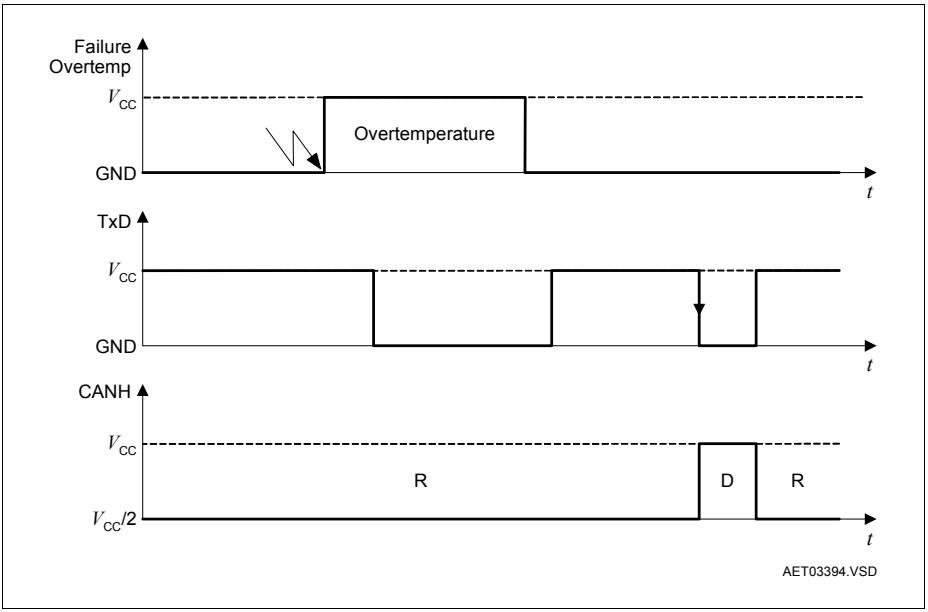


Figure 3 Release of the Transmission after Overtemperature

Reception

The analog CAN bus signals are converted into a digital signal at RxD via the differential input receiver.

In normal mode and RxD only, the split pin is used to stabilize the recessive common mode signal.

Permanent Recessive Clamping

If the RxD signal is permanent recessive, although there is a message sent on the bus, the host µC of this transceiver could start a message at any time, because the bus seems to be idle. To prevent this node to disturb the communication on the bus, the TLE 6251 G offers a so called permanent RxD recessive clamping. If the RxD signal is permanent recessive, an error flag is set and the transmitter is deactivated as long as the error occurs

Receive Only Mode (RxOnly Mode)

In the RxOnly mode, the transmission stage is deactivated but the reception of signals via the CAN bus is still possible. This mode is implemented to support hardware and software diagnosis functions.

If there is an hardware error on the transmission part of a node (e.g. bubbling idiot failure), in the RxOnly mode, the bus is no longer blocked and the µC can still receive the messages on the bus.

It is also possible to make a network analysis of the interconnections between the nodes. A connection between two nodes (in a network) is checked if both nodes are in the normal mode and all others are in RxOnly mode. If a message from one node is sent to the other, this has to be acknowledged. If there is no acknowledge of the message, the connection between the two nodes has an error.

The RxD pin also works as an diagnosis flag, which is described more in detail in **Table 2**.

Standby Mode

In the standby mode, transmission and reception of signals is deactivated. This is the first step of reducing the current consumption. The internal voltage regulator control pin (INH) is still active, so all external (INH controlled) powered devices are also activated.

Wake-Up

The wake-up is possible via WK-pin (filtering time $t > t_{WK}$) or CAN message (filtering time $t > t_{WU}$) and sets the RxD/NERR pins to LOW, see **Figure 4**. Now the µC is able to detect this change at RxD and switch the transceiver into the normal mode. Once the wake-up flag is set (= LOW), it remains in this state, as long as the transceiver is not transferred into the normal mode. The detection of the wake-up source is possible during the first 4 recessive to dominant edges at TxD in the normal mode.

Go-to Sleep Mode

The go-to sleep mode is used to have an intermediate step between the sleep mode and all other modes. This mode has to control if the sleep command (EN = 1, NSTB = 0) is activated for a minimum hold time $t > t_{hSLP}$. Afterwards the TLE 6251 G automatically transfers into the sleep mode. The activated features in go-to sleep mode are similar to the standby mode.

Sleep Mode

In the sleep mode, transmission and reception of signals is deactivated. This is the second step of reducing the current consumption. The internal voltage regulator control pin (INH) is deactivated.

Transition into other Modes during Sleep Mode

Transition from sleep into other modes is possible if V_{CC} and $V_{\mu C}$ active. Selection of the modes can be done by the mode control inputs.

Wake-Up

The wake-up is possible via WK-pin (filtering time $t > t_{WK}$) or CAN message (filtering time $t > t_{WU}$) and automatically transfers the TLE 6251 G into the standby mode and sets the RxD/NERR pins to LOW, see **Figure 4**. Once the TLE 6251 G has been set to the standby mode, the system voltage regulator is activated by the inhibit output INH, and the µC restarts. Now the µC is able to detect this change at RxD and switch the transceiver into the normal mode. Once the wake-up flag is set (= LOW), it remains in this state, as long as the transceiver is not transferred into the normal mode. The detection of the wake-up source is possible during the first 4 recessive to dominant edges at TxD in the normal mode.

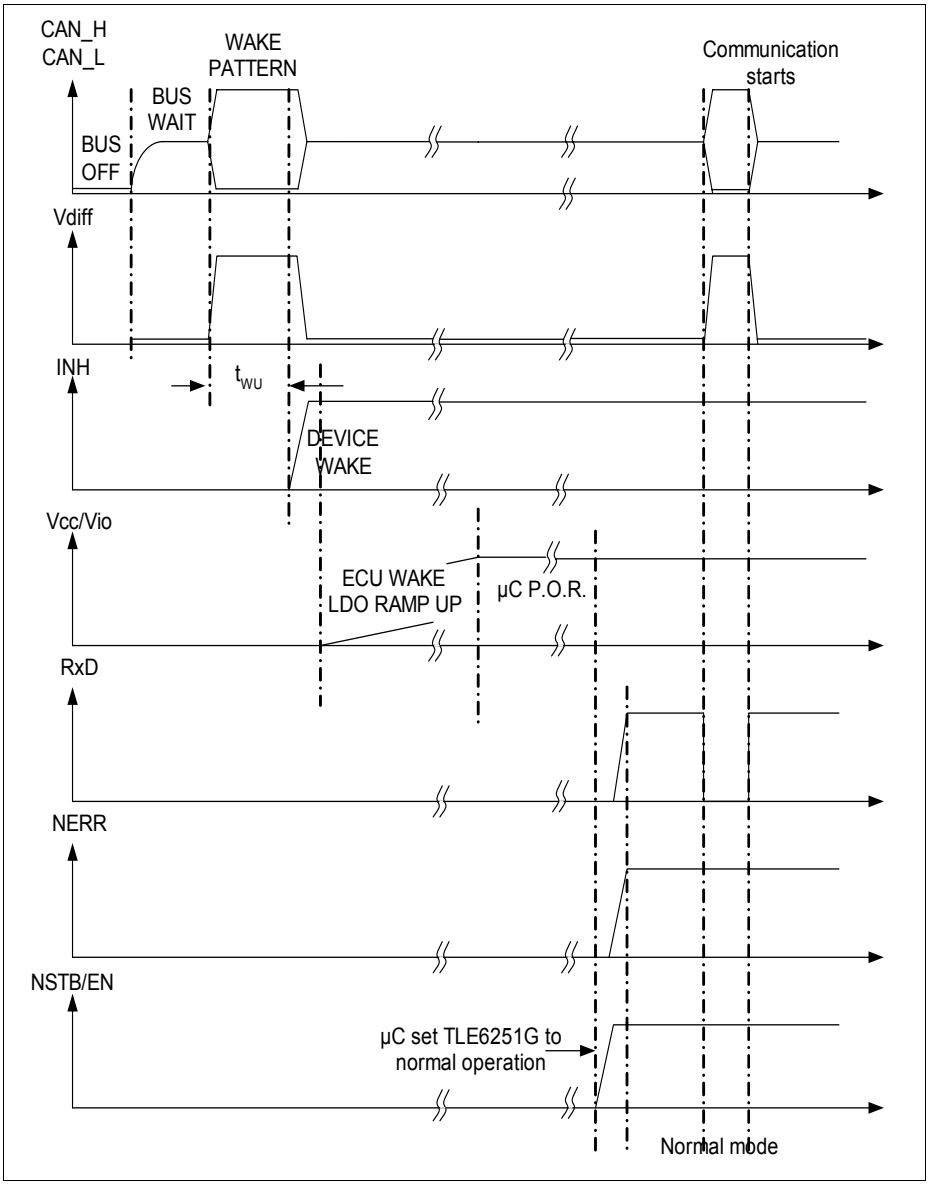


Figure 4 RxD during Sleep mode

Split Circuit

The split circuitry is activated during normal and RxOnly mode and deactivated (SPLIT pin high ohmic) during sleep and standby mode. The SPLIT pin is used to stabilize the recessive common mode signal in normal mode and RxOnly mode. This is realized with a stabilized voltage of 0.5 V_{CC} at SPLIT.

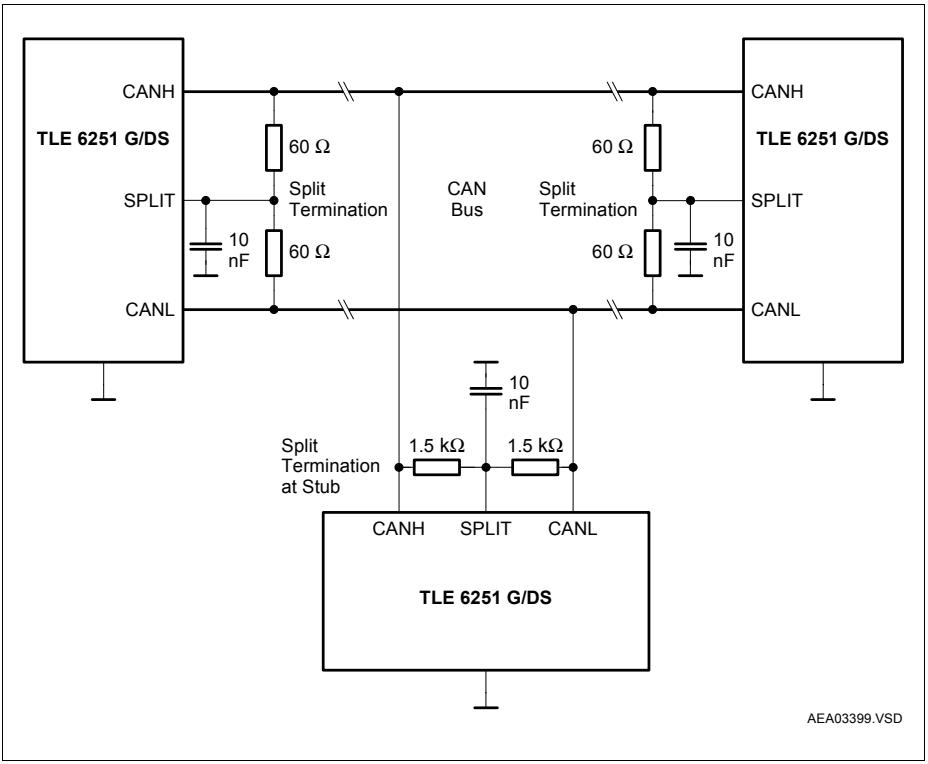


Figure 5 Application example for the SPLIT Pin

A correct application of the SPLIT pin is shown in **Figure 5**. The split termination for the left and right node is realized with two 60 Ω resistances and one 10 nF capacitor. The center node in this example is a stub node and the recommended value for the split resistances is 1.5 kΩ.

Diagnosis-Flags at NERR and RxD

Power-Up Flag

- Task: to signalize a power-up state at V_{BAT}

- Indicator: NERR = LOW in RxOnly mode
- Remarks: Power-up flag is cleared when entering the normal mode

Wake-Up Flag

- Task: to signalize a wake-up condition at the WK pin (filtering time $t > t_{WK}$) or via CAN bus message (filtering time $t > t_{WU}$)
- Indicator: RxD or NERR = LOW in sleep/stand-by mode immediately after wake-up
- Remarks: Flag is cleared on entering the RxOnly mode

Wake-Up Source Flag

- Task: to distinguish between the two wake-up sources
- Indicator: NERR = LOW in normal mode = wake-up via WK pin
- Remarks: only available if the power-up flag is cleared. After four recessive to dominant edges on TxD in normal mode, the flag is cleared. Leaving the normal mode clears the wake-up source flag.

Bus Failure Flag

- Task: to signalize a bus line short circuit condition to GND, V_S or V_{CC}
- Indicator: NERR = LOW in normal mode
- Remarks: flag is set after four consecutive recessive to dominant cycles on pin TxD when trying to drive the bus dominant. The bus failure flag is cleared if the normal mode is reentered or 4 recessive to dominant edges at TxD without failure condition.

Local Failure Flag

- Task: to signalize one of the five local failure conditions described in **Local Failure-Flags and -Detection**
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Remarks: the flag is cleared when entering the normal mode from RxOnly mode or when RxD is dominant while TxD is recessive.

Local Failure-Flags and -Detection

TxD Dominant Failure Detection

- Effect: permanent dominant signal for $t > t_{TxD}$ at TxD
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Action: disabling of the transmitter stage
- Remarks: release of the transmitter stage only after transition into RxOnly mode (failure diagnosis) and transition into normal mode.

RxD Permanent Recessive Clamping

- Effect: internal RxD signal does not match signal at RxD pin because the RxD pin is pulled to HIGH (permanent HIGH)
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Action: disabling of the receiver stage
- Remarks: the flag is cleared by changing from RxOnly (failure diagnosis) into normal mode or RxD gets dominant.

TxD to RxD Short Circuit

- Effect: short circuit between RxD and TxD
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Action: disabling of the transmitter stage
- Remarks: the flag is cleared by changing from RxOnly (failure diagnosis) into normal mode.

Bus Dominant Clamping

- Effect: permanent dominant signal at the CAN bus for $t > t_{BUS}$
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Action: none
- Remarks: none

Overtemperature Detection

- Effect: junction temperature at the driving stages exceeded
- Indicator: NERR = LOW in RxOnly mode (local failure flag is set)
- Action: disabling of the transmitter stage
- Remarks: the flag is cleared by changing from RxOnly (failure diagnosis) into normal mode or RxD gets dominant. Bus only released after the next dominant bit in TxD.

Other Features

$V_{\mu C}$-level Adapter

The advantage of the adaptive µC logic is the ratiometrical scaling of the I/O levels depending on the input voltage at the $V_{\mu C}$ pin. So it can be ensured that the I/O voltage of the µC fits to the internal logic levels of the TLE 6251 G.

WAKE Input

The wake-up input pin is a bi-level sensitive input. This means that both transitions, HIGH to LOW and LOW to HIGH, result in a wake-up.

V_{CC}, $V_{\mu C}$ Undervoltage Detection

If an undervoltage condition at V_{CC}, $V_{\mu C}$ is detected for longer than $t = t_{UV,t}$, the TLE 6251 G automatically transfers into the sleep mode and the undervoltage flag is set. This flag is an internal flag and not available via NERR or RxD. The flag is cleared again, after setting the power on or wake flag (power-up or wake-up).

V_S Undervoltage Detection

If an undervoltage condition at V_S is detected, the TLE 6251 G immediately transfers into the standby mode and the undervoltage flag is set. This flag is an internal flag and not available via NERR or RxD. The flag is cleared again, after the supply voltage V_S has reached the nominal value.

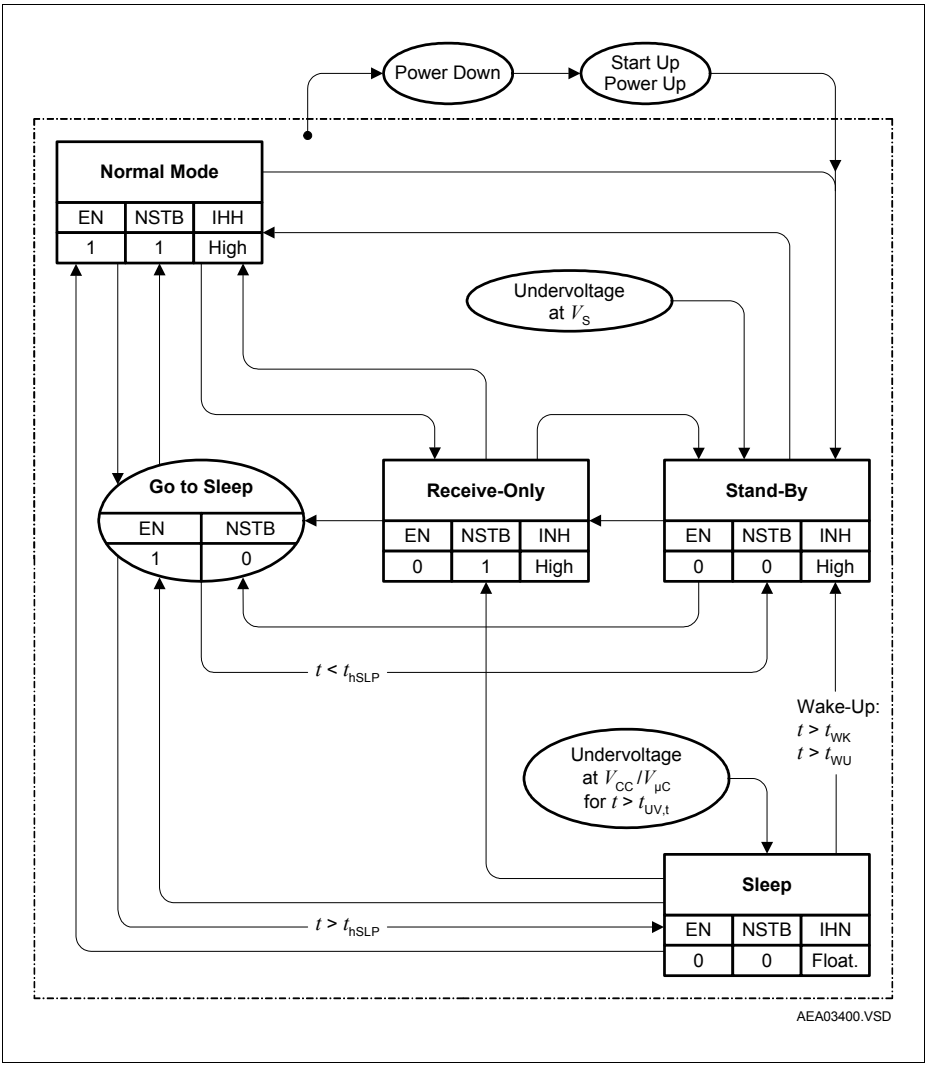


Figure 6 Mode State Diagram

Table 2 Truth Table

NSTB	EN	INH	Mode	Event	NERR	RxD	SPLIT
1	1	HIGH	NORMAL	No CAN bus failure[1)]	1	LOW: bus dominant, HIGH: bus recessive	ON
				CAN bus failure[1)]	0		
				CANH/CANL driver off[2)]	1		
				Wake-up via CAN bus/no wake-up request detected	1		
				Wake-up via pin WK[3)]	0		
1	0	HIGH	RECEIVE ONLY	No V_{BAT} fail detected[4)]	1	LOW: bus dominant, HIGH: bus recessive	ON
				V_{BAT} fail detected[4)]	0		
				No TxD time-out, overtemperature, RxD recessive clamping or bus dominant time out detected[5)]	1		
				TxD time-out, overtemperature, RxD recessive clamping or bus dominant time out detected[5)]	0		
0	0	HIGH	STAND BY	Wake-up request detected[6)]	0	0	OFF
				No Wake up request detected[6)]	1	1	
0	1	HIGH[7)]	GO TO SLEEP	Wake-up request detected[6)]	0	0	OFF
				No wake-up request detected[6)]	1	1	
0	0	floating	SLEEP[8)]	Wake-up request detected[6)]	0	0	OFF
				No wake-up request detected[6)]	1	1	

1) Only valid AFTER at least four recessive to dominant edges at TxD after entering the normal mode.

2) Due to an thermal overtemperature shutdown or TxD time-out.

3) Only valid BEFORE four recessive to dominant edges at TxD after entering the normal mode.

4) Power on situation, valid if V_{CC} and $V_{\mu C}$ is active and transition from sleep, stand-by or goto sleep command.

5) Transition from normal mode.

6) Only valid if V_{CC} and $V_{\mu C}$ are active.

7) If this mode is selected for a time longer than the hold time of the go-to sleep command ($t > t_{hSLP}$), INH is floating.

8) Transition into the sleep mode only if go-to sleep command was selected for a time longer than the hold time of the go-to sleep command ($t > t_{hSLP}$).

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_S	-0.3	40	V	–
5 V supply voltage	V_{CC}	-0.3	5.5	V	–
Logic supply voltage	$V_{\mu C}$	-0.3	5.5	V	–
CAN bus voltage (CANH, CANL)	$V_{CANH/L}$	-27	40	V	–
Differential voltage CANH, CANL, SPLIT, WK	$V_{diffESD}$	-40	40	V	CANH - CANL < |40 V|; CANH - SPLIT < |40 V| CANL - SPLIT < |40 V|; CANL - WK < |40 V|; CANH - WK < |40 V|; Split - WK < |40 V|
V_{SPLIT} input voltage	V_{SPLIT}	-27	40	V	–
Input voltage at WK	V_{WK}	-27	40	V	–
Input voltage at INH	V_{INH}	-0.3	V_S + 0.3	V	–
Logic voltages at EN, NSTB, NERR, TxD, RxD	V_I	-0.3	$V_{\mu C}$	V	0 V < $V_{\mu C}$ < 5.5 V
Electrostatic discharge voltage at SPLIT	V_{ESD}	-1	1	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage at CANH, CANL, WK vs. GND	V_{ESD}	-6	6	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage for all pin except SPLIT	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage at CANH, CANL vs. GND	V_{ESD}	-6	6	kV	According to IEC61000-4-2 (150 pF via 330Ω) See **Figure 10**[1)]
Temperatures					
Storage temperature	T_j	-40	150	°C	–

1) application circuits with and without terminated SPLIT pin

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_S	5	40	V	–
5 V supply voltage	V_{CC}	4.75	5.25	V	–
Logic supply voltage	$V_{\mu C}$	3.0	5.25	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances					
Junction ambient	$R_{thj\text{-}a}$	–	120	K/W	1)
Thermal Shutdown (junction temperature)					
Thermal shutdown temp.	T_{jSD}	150	190	°C	–
Thermal shutdown hyst.	ΔT	–	10	K	–

1) Calculation of the junction temperature $T_j = T_{amb} + P \times R_{thj\text{-}a}$

Table 5 Electrical Characteristics

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current Consumption						
Current consumption normal mode	$I_{CC+\mu C}$	–	6	10	mA	recessive state; TxD = high
	$I_{CC+\mu C}$	–	50	80	mA	dominant state; TxD = low
Current consumption RxD Only mode	$I_{CC+\mu C}$	–	6	10	mA	receive only mode
Current consumption stand-by mode	I_{VS}	–	25	50	µA	stand-by mode; V_S = WK = 12 V
	$I_{CC+\mu C}$	–	25	60	µA	stand-by mode; V_S = WK = 12 V V_{CC} = $V_{\mu C}$ = 5V
Current consumption sleep mode	I_{VS}	–	25	35	µA	sleep mode, V_S = 12 V, T_j < 85 °C, V_{CC} = $V_{\mu C}$ = 0 V
	$I_{CC+\mu C}$	–	2.5	10	µA	sleep mode, V_S = 12 V, T_j < 85 °C, V_{CC} = $V_{\mu C}$ = 5V
Supply Resets						
V_{CC} undervoltage detection	$V_{CC,UV}$	2	3	4	V	–
$V_{\mu C}$ undervoltage detection	$V_{\mu C,UV}$	0.4	1.2	1.8	V	–
V_S power ON detection level	$V_{S,Pon}$	2	4	5	V	–
V_S power OFF detection level	$V_{S,Poff}$	2	3.5	5	V	–
Receiver Output RxD						
HIGH level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RD} = 0.8 × $V_{\mu C}$
LOW level output current	$I_{RD,L}$	2	4	–	mA	V_{RD} = 0.2 × $V_{\mu C}$
Short circuit current	$I_{SC,RxD}$	–	70	84	mA	$V_{\mu C}$ = 5.25 V, RxD = LOW

Table 5 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Short circuit current	$I_{SC,RxD}$	–	35	45	mA	$V_{\mu C}$ = 3.3 V, RxD = LOW

Table 5 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TD,H}$	–	0.52× $V_{\mu C}$	0.7 × $V_{\mu C}$	V	recessive state
LOW level input voltage threshold	$V_{TD,L}$	0.30× $V_{\mu C}$	0.48× $V_{\mu C}$	–	V	dominant state
TxD input hysteresis	$V_{TD,hys}$	100	400	1000	mV	Not subject to production test Specified by design.
HIGH level input current	I_{TD}	-5	0	5	µA	$V_{TxD} = V_{\mu C}$
TxD pull-up resistance	R_{TD}	10	20	40	kΩ	–
Mode Control Inputs EN, NSTB						
HIGH level input voltage threshold	$V_{M,H}$	–	0.52× $V_{\mu C}$	0.7 × $V_{\mu C}$	V	–
LOW level input voltage threshold	$V_{M,L}$	0.30× $V_{\mu C}$	0.48× $V_{\mu C}$	–	V	–
Input hysteresis	$V_{M,hys}$	100	400	1000	mV	Not subject to production test Specified by design.
LOW level input current	I_{MD}	-5	0	5	µA	V_{EN} / V_{NSTB} = 0V
Pull-down resistance	R_M	10	20	40	kΩ	–
Diagnostic Output NERR						
HIGH level output voltage	$V_{NERR,H}$	0.8 × $V_{\mu C}$	–	–	V	I_{NERR} = -100 µA
LOW level output voltage	$V_{NERR,L}$	–	–	0.2 × $V_{\mu C}$	V	I_{NERR} = 1.25 mA
Short circuit current	$I_{SC,NERR}$	–	20	48	mA	$V_{\mu C}$ = 5.25 V
Short circuit current	$I_{SC,NERR}$	–	13	25	mA	$V_{\mu C}$ = 3.3 V

Table 5 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Termination Output SPLIT						
Split output voltage	V_{SPLIT}	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V	normal mode; -500 µA < I_{SPLIT} < 500 µA
	V_{SPLIT}	0.45× V_{CC}	0.5 × V_{CC}	0.55× V_{CC}	V	normal mode; no load
Leakage current	I_{SPLIT}	-5	0	5	µA	sleep mode V_{CC} = $V_{\mu C}$ = 0 V
Output resistance	R_{SPLIT}	–	600	–	Ω	–
Wake Input WK						
Wake-up threshold voltage	$V_{WK,th}$	V_S - 4	V_S - 2.5	V_S - 2	V	V_{NSTB} = 0 V
HIGH level input current	I_{WKH}	–	5	10	µA	V_{WK} = $V_{WK,th}$ + 1
LOW level current	I_{WKL}	-10	-5	–	µA	V_{WK} = $V_{WK,th}$ - 1
Inhibit Output INH						
HIGH level voltage drop ΔV_H = V_S - V_{INH}	ΔV_H	–	0.4	0.8	V	I_{INH} = -1 mA
Leakage current	$I_{INH,lk}$	–	–	5	µA	sleep mode; V_{INH} = 0 V
Bus Transmitter						
CANL/CANH recessive output voltage	$V_{CANL/H}$	2.0	–	3.0	V	no load
CANH, CANL recessive output voltage difference	V_{diff}	-500	–	50	mV	V_{TxD} = $V_{\mu C}$; no load
CANL dominant output voltage	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V;
CANH dominant output voltage	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V
CANH, CANL dominant output voltage difference	V_{diff}	1.5	–	3.0	V	V_{TxD} = 0 V

Table 5 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
CANL short circuit current	I_{CANLsc}	50	80	200	mA	$V_{CANLshort}$ = 18 V
CANH short circuit current	I_{CANHsc}	-200	-80	-50	mA	$V_{CANHshort}$ = 0 V
Leakage current	$I_{CANHL,lk}$	-5	0	5	µA	$V_S = V_{\mu C} = V_{CC}$ = 0 V; 0 V < $V_{CANH,L}$ < 5 V
Bus Receiver						
Differential receiver threshold voltage, normal mode	$V_{diff,rdN}$	–	0.8	0.9	V	see CMR
	$V_{diff,drN}$	0.5	0.6	–	V	see CMR
Differential receiver threshold, low power mode	$V_{diff,rdLP}$		0.9	1.15	V	recessive to dominant
	$V_{diff,drLP}$	0.4	0.8		V	dominant to recessive
Common Mode Range	CMR	-12	–	12	V	V_{CC} = 5 V
Differential receiver hysteresis	$V_{diff,hys}$	–	200	–	mV	–
CANH, CANL input resistance	R_i	10	20	30	kΩ	recessive state
Differential input resistance	R_{diff}	20	40	60	kΩ	recessive state
Dynamic CAN-Transceiver Characteristics						
Min. hold time go to sleep command	t_{hSLP}	8	25	50	µs	–
Min. wake-up time on pin WK	t_{WK}	5	10	20	µs	–
Min. dominant time for bus wake-up	t_{WU}	0.75	3	5	µs	–
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC} = V_{\mu C}$ = 5 V; C_{RxD} = 15 pF

Table 5 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < $V_{\mu C}$ < 5.25 V; 6.0 V < V_S < 40 V; R_L = 60 Ω; normal mode; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	C_L = 47 pF; R_L = 60 Ω; V_{CC} = $V_{\mu C}$ = 5 V; C_{RxD} = 15 pF
Propagation delay TxD LOW to bus dominant	$t_{d(L),T}$	–	50	105	ns	C_L = 47 pF; R_L = 60 Ω; V_{CC} = $V_{\mu C}$ = 5 V
Propagation delay TxD HIGH to bus recessive	$t_{d(H),T}$	–	50	105	ns	C_L = 47 pF; R_L = 60 Ω; V_{CC} = $V_{\mu C}$ = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	50	150	ns	C_L = 47 pF; R_L = 60 Ω; V_{CC} = $V_{\mu C}$ = 5 V; C_{RxD} = 15 pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	100	150	ns	C_L = 47 pF; R_L = 60 Ω; V_{CC} = $V_{\mu C}$ = 5 V; C_{RxD} = 15 pF
TxD permanent dominant disable time	t_{TxD}	0.3	0.6	1.0	ms	–
Bus permanent time-out	$t_{Bus,t}$	0.3	0.6	1.0	ms	–
V_{CC}, $V_{\mu C}$ undervoltage filter time	$t_{UV,t}$	50	80	120	ms	–

Diagrams

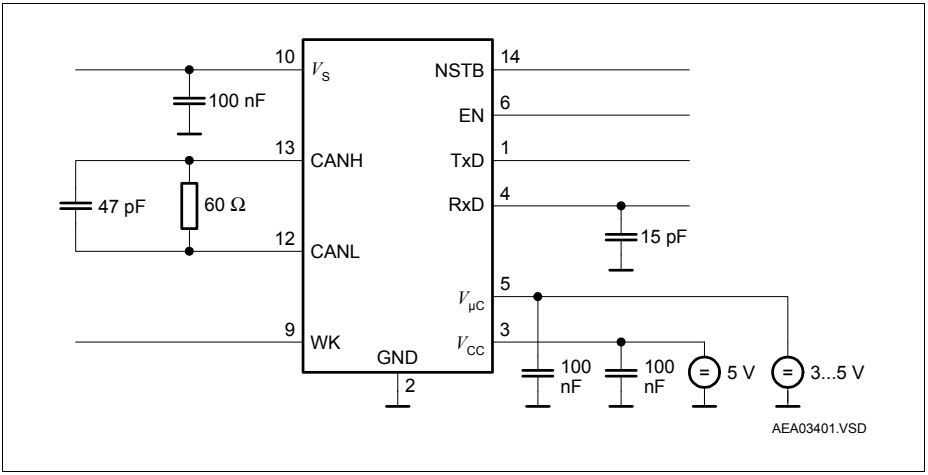


Figure 7 Test Circuit for Dynamic Characteristics

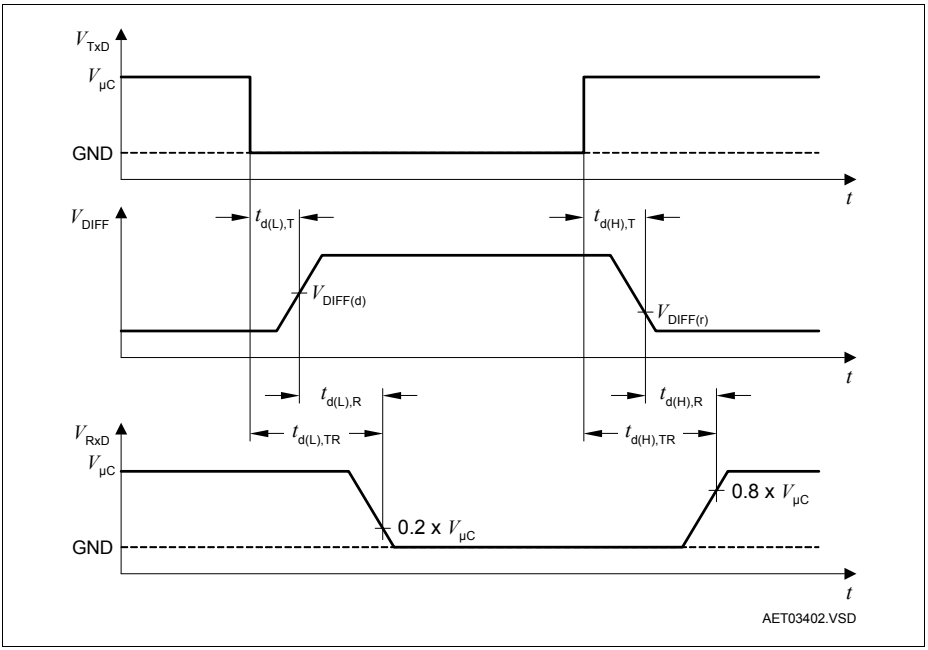


Figure 8 Timing Diagrams for Dynamic Characteristics

Application

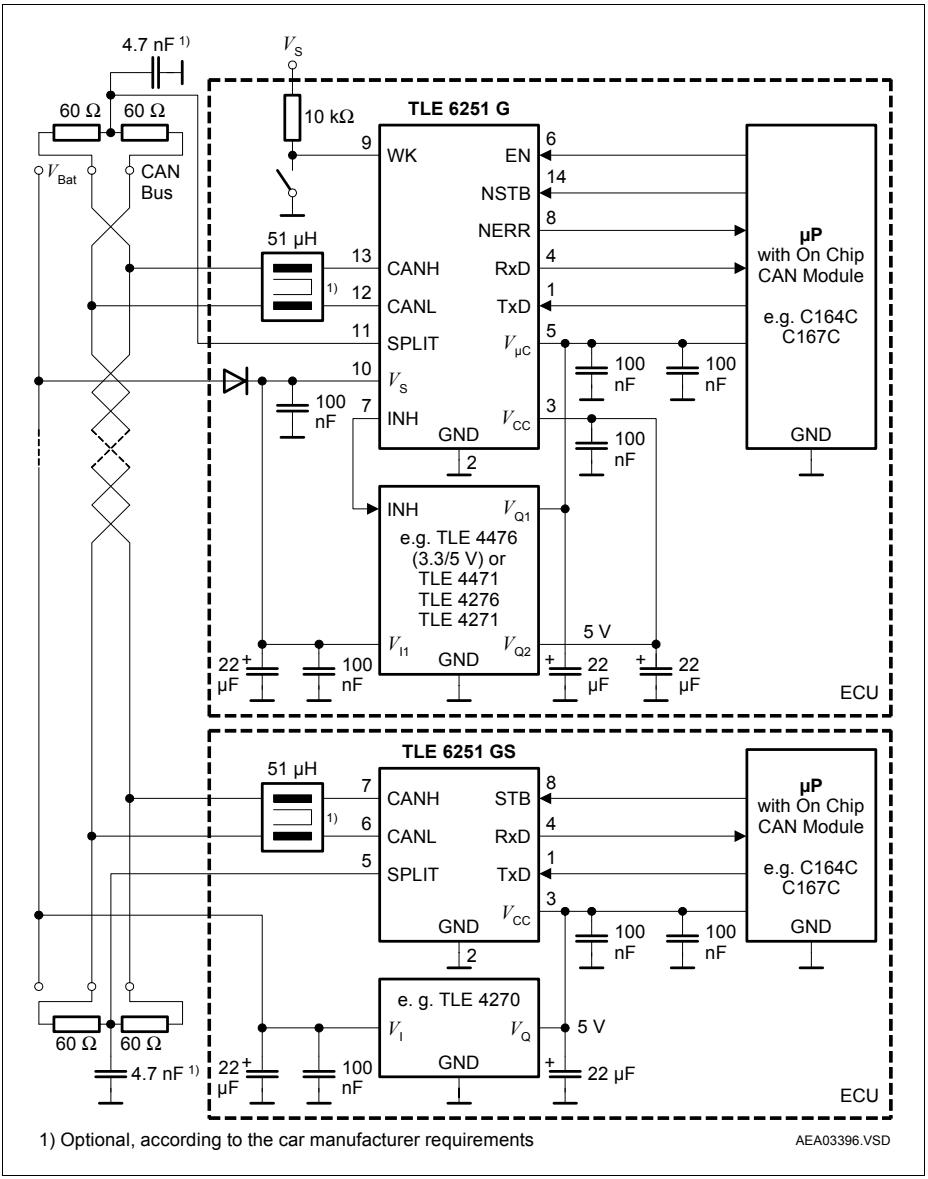


Figure 9 Application Circuit Example

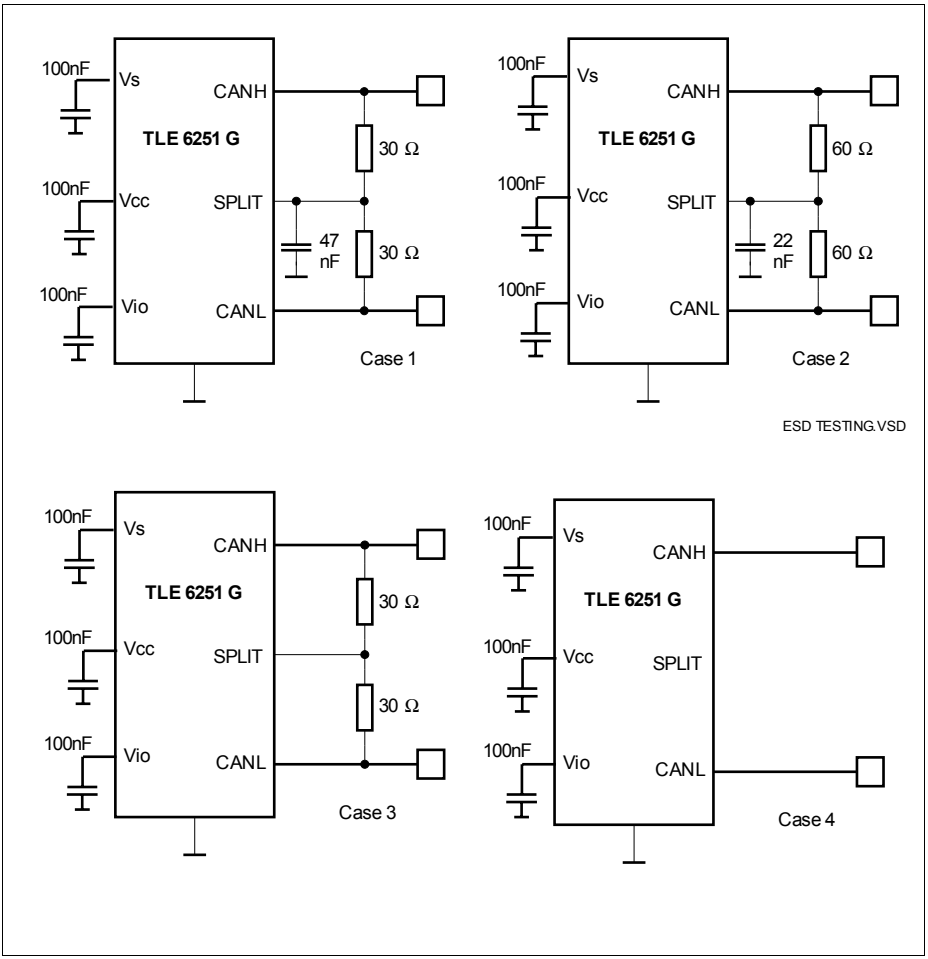
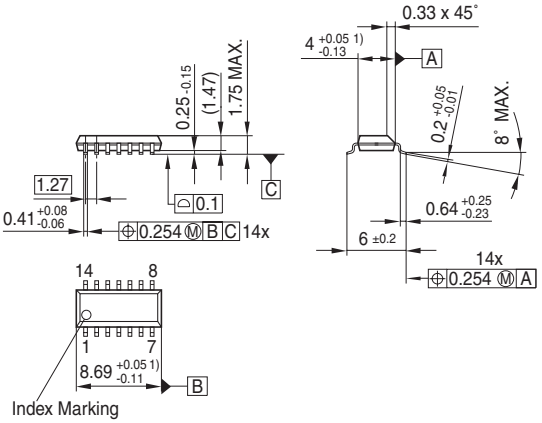


Figure 10 ESD test for conformance to IEC 61000-4-2

The 100nF decoupling capacitors on Vs, Vio and Vcc are situated 5mm from the pins.

The distance between the fixpoint where the Gun is applied and the pin CAN_H and CAN_L are 20mm. The test has been realized with NoiseKen ESS2000.

Package Outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPS09330

Figure 11 **P-DSO-14-13** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 3.3	2008-06-19	Initial version Rev 3.2. Ordering Code outdated! Page 3: Change Ordering code to: “On Request”